within the hub; and

sending the processed information without modification over at least one of the communication links to at least one of the first and second processors associated with the at least one destination address, thereby defining at least one addressed processor.

8. A method as set forth in claim 1 wherein the step of indexing the first and second processors is further defined as indexing the processors to define a different code for each of the processors for differentiating the processors.

19. A distributed multiprocessing system comprising;

a first processor for processing information at a first station and for assigning a first address to a first processed information,

a second processor for processing information at a second station and for assigning a second address to a second processed information,

a central signal routing hub,

an indexer connected to said routing hub for indexing said first and second processors to define different destination addresses for each of said processors,

a first communication link interconnecting said first processor and said hub for transmitting said first processed information between said first processor and said hub;

a second communication link interconnecting said second processor and said hub for transmitting said second processed information between said second processor and said hub,

said central routing hub including a sorter for receiving at least one of said first and second processed information from at least one of said first and second processors, thereby defining at least one sending processor, and for associating a destination of at least one of said first and second addresses of said first and second processed information, respectively, with at least one of said destination addresses, and for sending at least one of said first and second processed information without modification over at least one of said communication links to at least one of said first and second processors associated with said destination address, thereby defining at least one addressed

R3

processor.

W4

27. A system as set forth in claim 19 wherein said indexer defines a different code for each of said processors for differentiating said processors.